METHODS OF FORMING METAL LAYERS IN INTEGRATED CIRCUIT DEVICES USING SELECTIVE DEPOSITION ON EDGES OF RECESSES AND CONDUCTIVE CONTACTS SO FORMED

ABSTRACT

Methods of forming a metal layer in integrated circuit devices using selective electroplating in a recess are disclosed. In particular, a recess is formed in a surface of an insulating layer. The recess has a side wall inside the recess, a bottom inside the recess, and an edge at a boundary of the surface of the insulating layer and the side wall. A selective electroplating mask is formed on the side wall to provide a covered portion of the side wall and an exposed portion of the side wall. The exposed portion of the side wall can be electroplated with a metal. Related conductive contacts are also disclosed.